Outlier control technology and feedforward lithography can boost FOPLP yield

Fan-out panel level packaging (FOPLP) has many advantages, but the critical challenge of die placement error can substantially impact yields and costs. The experts at Onto Innovation describe how they are helping solve the problem for customers by substantially increasing both yield and throughput.

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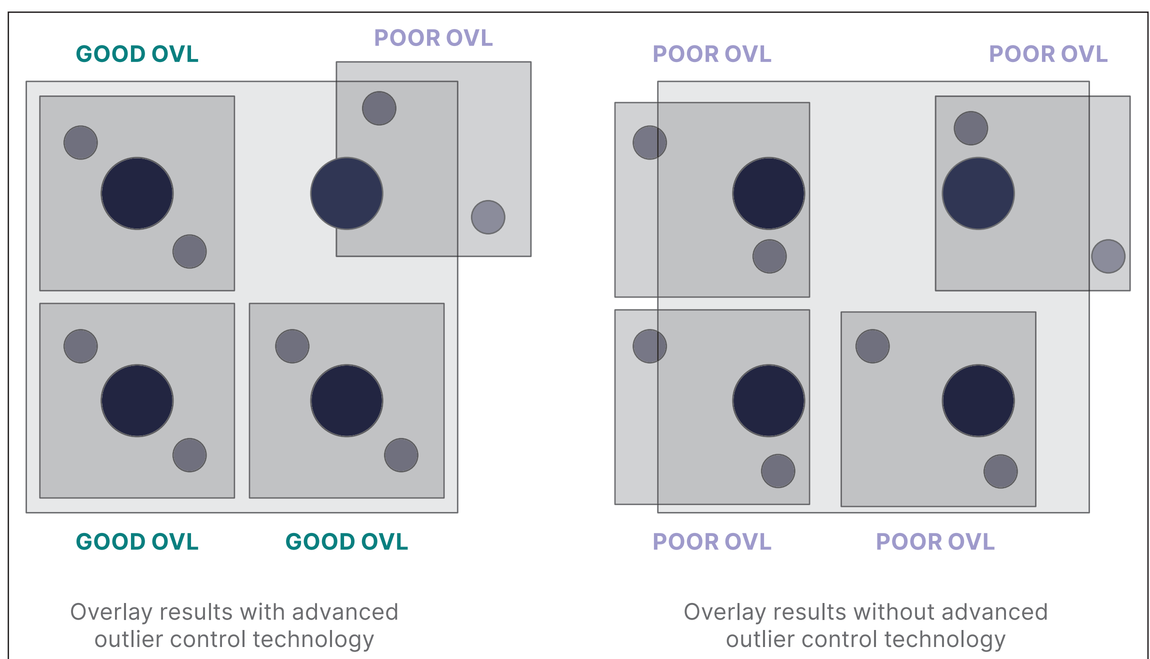
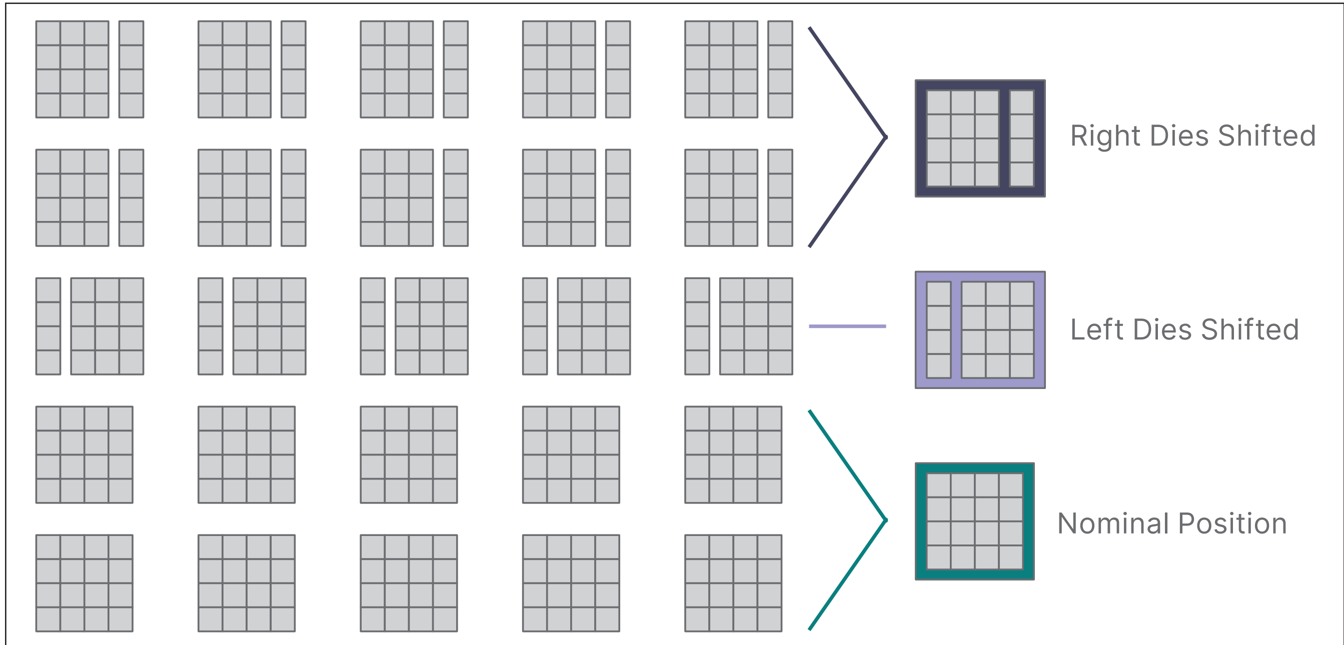
FAN-OUT PANEL LEVEL PACKAGING (FOPLP) has multiple benefits in advanced packaging applications, including enhanced connectivity and reduced costs. FOPLP differs from wafer-level packaging processes in that FOPLP utilizes large, rectangular panels rather than the round silicon wafers typically associated with IC manufacture. FOPLP's rectangular panels more efficiently fit rectangular die, which can reduce costs since manufacturers can process more packages in each run.

Despite many advantages, FOPLP also faces specific challenges, such as yield loss caused by inaccurate die placement and the resulting overlay errors. In this context, dies with unusually large placement errors, or outliers, can be especially troublesome.

These outliers cause losses of both the misplaced die and surrounding dies. However, integrating outlier control with feedforward metrology can greatly improve both yield and throughput.



➤ Figure 1. Outliers with large placement errors can cause unacceptable overlay errors, but excluding outliers from the correction calculation preserves the remaining dies.

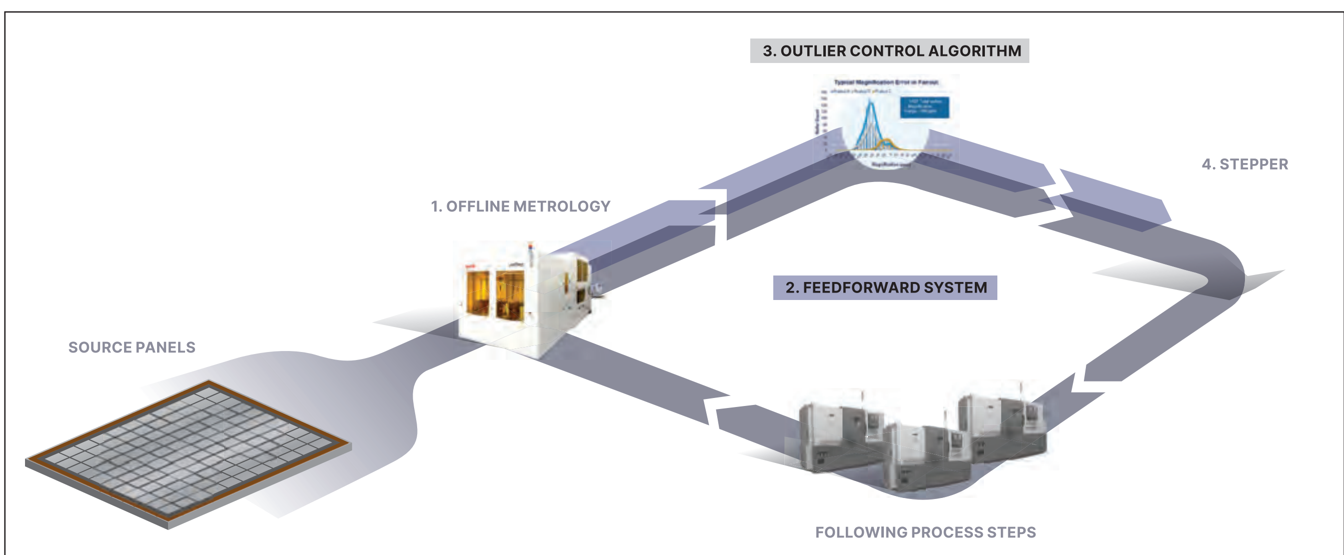


➤ Figure 2. The die clusters in the first three rows included intentional placement errors: in the first two rows, the rightmost column of each die cluster was shifted 100μm to the right; in the third row, the leftmost column of each die cluster was shifted 100μm to the left. The fourth and fifth rows did not include intentional errors.

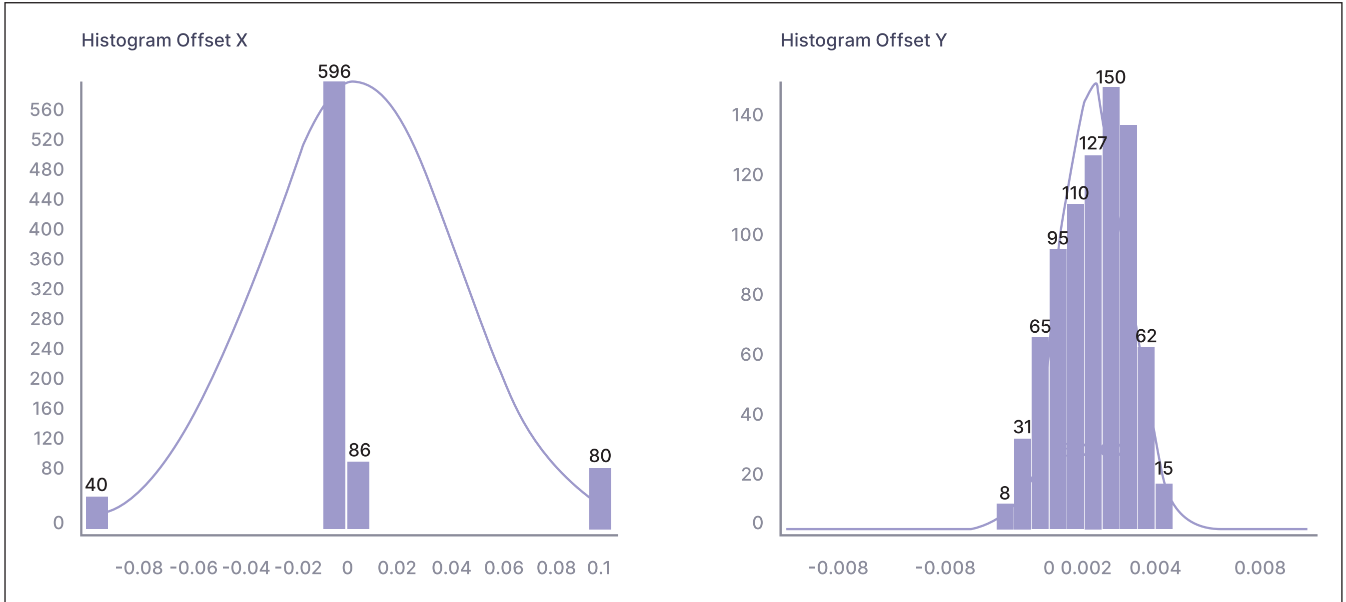
Fan-out processes cut individual dies from the wafer and reconstitute them on a processing substrate separated by additional space. Subsequent steps fabricate redistribution lines in multiple layers and end with the creation of contacts on the surface of the package. The area available for contacts is increased by the additional space between chips, allowing more contacts per chip.

One critical challenge for FOPLP is die-placement error. This error originates during the robotic pick-and-place operation in which chips are positioned on the reconstitution substrate. The problem arises when die positions shift during subsequent processing steps. If uncorrected, these die-placement errors can result in overlay errors and reduced yield.

While die-placement errors can be measured and corrected, die-by-die in the lithography tool, this greatly reduces throughput. Feedforward lithography, which measures placement errors and calculates corrections in a separate system and then feeds



➤ Figure 3. Feedforward lithography and advanced outlier technology integrated in a FOPLP process. 1) A panel is processed by an offline metrology tool. 2) The metrology data is fed forward to the outlier control algorithm. 3) The outlier control algorithm identifies the outliers. 4) The processed metrology data is fed forward to the lithography tool for site-by-site or die-by-die exposure corrections.

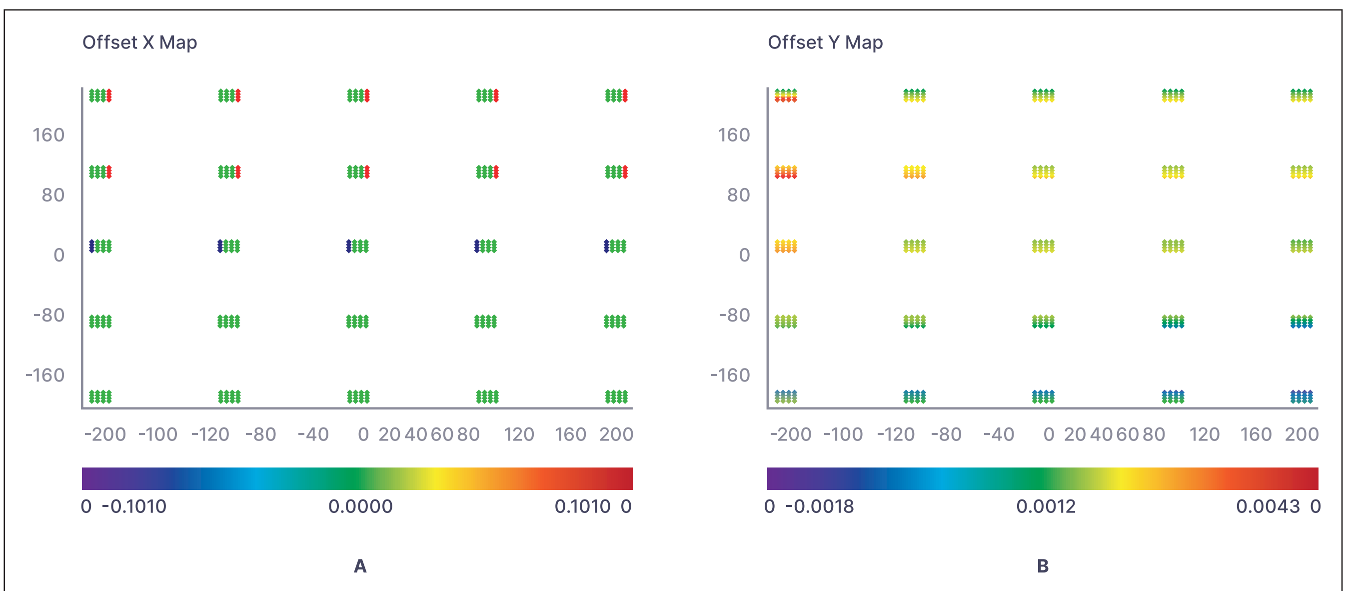


➤ Figure 4. (left). The X placement deviation histogram shows most die having little error and some die with +100μm and -100μm errors, which matched the designed die errors of the test panel. The Y placement deviation histogram shows a small range (+4μm to -2μm), as expected.

the corrections forward to the lithography system, is much faster. Lithography throughput can be further increased by including more than one die in each exposure site and then applying site-by site corrections to the exposures.

In this scheme, dies with unusually large placement errors can have an outsized impact on yields by skewing the site correction to such a degree that the site correction causes unacceptable overlay errors for all dies in the site. A solution: advanced outlier control technology (Figure 1). This technology detects outliers and excludes them from the correction calculation, thereby sacrificing the outlier to optimize overall yield and throughput.

Onto Innovation evaluated the use of advanced outlier control technology with feedforward lithography on a test panel. The test panel included intentionally displaced dies with large known placement errors. In the evaluation, integrating site-by-site exposure, offline feedforward metrology and advanced outlier control significantly improved both yield and throughput. To demonstrate the benefit of site-by-site exposure, offline feedforward metrology and advanced outlier control, these technologies were evaluated using



➤ Figure 5. (a) Heat map of die error in X axis. The right dies in the first two rows (red) have +100μm error. Left dies in the third row (blue) have -100μm error, reflecting intentional errors in test panel. (b) Heat map of die errors in Y axis. All the die errors are within -2μm to 4μm. No large Y axis errors are seen within clusters.

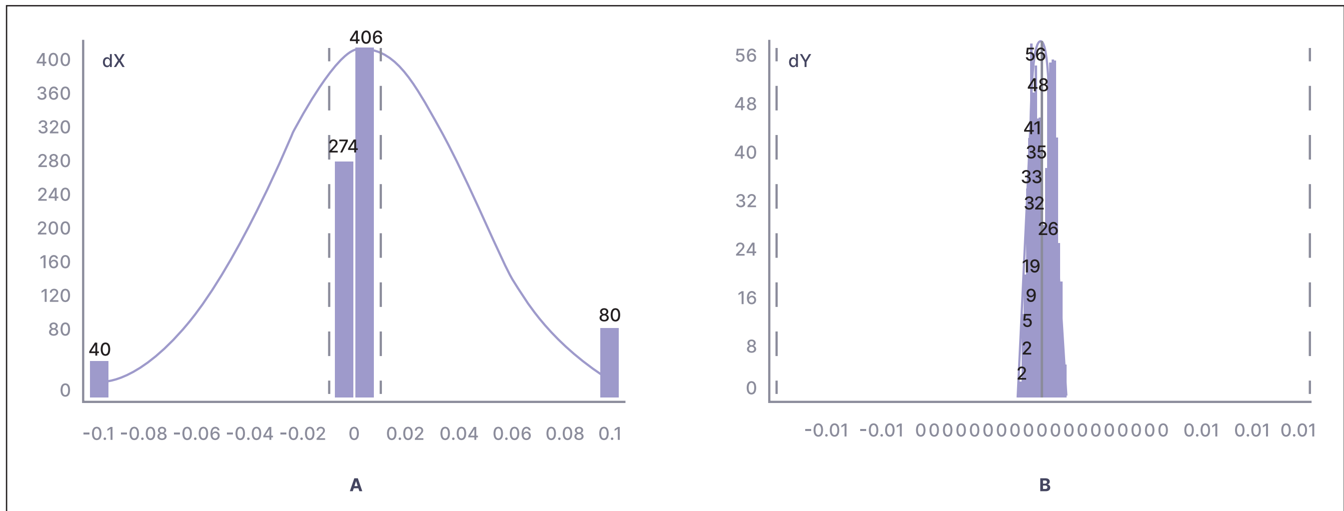


Figure 6. (a) Predicted residue values in X: two groups are observed at ±100µm from the designed outliers. The rest of the data points are within ±3µm. (b) Predicted residue values in Y axis: all the predicted residue values are within ±2µm, which matches expectations.

a 510mm x 515mm test panel containing 400 dies (Figure 2). The dies were grouped in 25 clusters arranged in a 5 x5 array across the panel. Each cluster contained 16 die in a 4 x4 array and was included in a single exposure site. A site correction was calculated from the individual placement errors measured for the included dies and then applied to each exposure.

The die clusters in the first three rows included intentional placement errors: in the first two rows, the rightmost column of each die cluster was shifted 100µm to the right. In the third row, the leftmost column of each die cluster was shifted 100µm to the left. The fourth and fifth rows provided a control group that did not include intentional errors. Without advanced outlier control technology, researchers expected all dies in the first three rows to suffer poor overlay when using site-by-site exposure.

Test panel placement errors were measured using an offline metrology tool that analyzed the measurements to identify outliers. The outlier threshold was set to 15µm. Dies with placement errors that exceeded the threshold were marked, and their information was discarded during the correction calculation. The correction data were fed forward to the stepper and used in the site-by-site exposure process.

Figure 3 shows the working scenario of feedforward lithography and advanced outlier technology.

Researchers used an Onto Innovation JetStep® 3500 Lithography System. This system supports up to 720mm x 600mm glass panels or up to 510mm x 515mm copper clad laminate (CCL) substrates. The optical system has a 2:1 magnification and an exposure field of up to 59mm x 59mm. The system can achieve 2µm resolution with ±400ppm magnification compensation. Compensation is required in a fan-out process to correct the die errors.

The lithography tool's pattern recognition system can be trained to use a unique pattern within the field of view as an alignment site and measure the X and Y positions of patterns across the panel. This enables local die-by-die exposure and site-by-site exposure capability without the use of offline metrology. The system can also accept feedforward corrections from an offline metrology tool, as evaluated in this study.

The Onto Innovation Firefly® automated optical inspection (AOI) system was utilized for the offline measurement of die-placement errors for feedforward metrology. This tool supports up to a 510mm x 515mm substrate.

Adding outlier control technology and feedforward lithography increases throughput to 62.7 panels per hour and yield to 85%. The numbers will vary for different processes, but feedforward lithography and outlier control offer significant improvements in yield and throughput in this evaluation

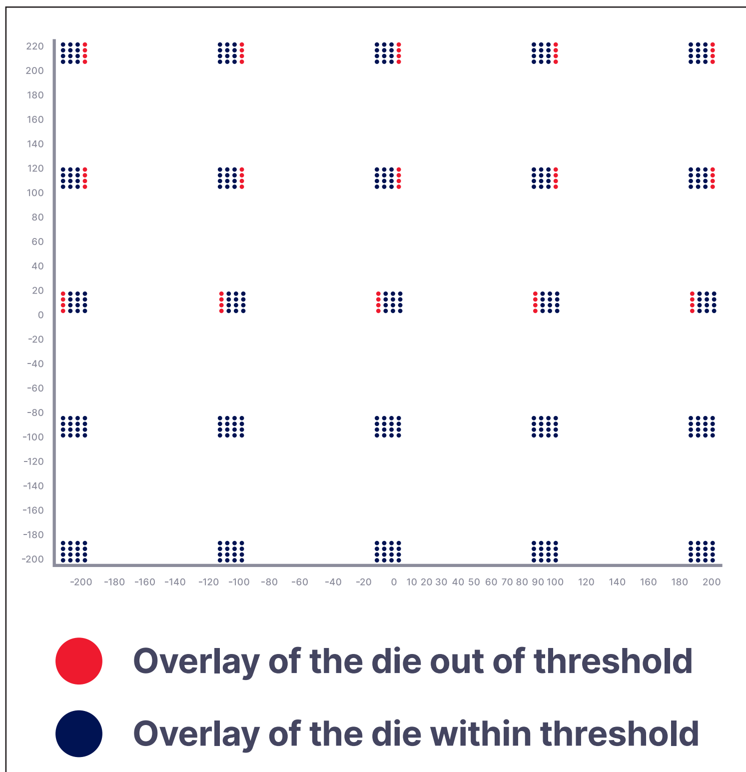
Ef Num	Yield	Offset Threshold	Outlier Shot Num	Outlier Point Num
min		min	min	
25.0000	0.8500	0.0150	0.0000	120.0000

➤ Figure 7. Predicted yield of the test panel is 85%. Yield prediction is a feature of the feedforward system used in this study. The overlay threshold is set to ±15 µm.

In the feedforward operation, die location and error data are automatically sent to the outlier algorithm and the stepper.

Results

Figure 4 shows the die-error histogram of the metrology data from the offline metrology tool. The left side of Figure 4 shows the placement deviation of the dies on the test panel in the X direction. The maximum X deviation was around +100µm, and the minimum X deviation was around -100µm, which matched the die errors that were designed into the test panel. The right side of Figure 4 shows the placement deviation of dies in the Y direction. The Y deviation range was from -2µm to +4µm, which was normal and expected.



➤ Figure 8. Heat map created by an offline metrology tool of actual overlay results for the test panel: the distribution of good and bad die overlays matched the design layout and expectation with outlier control enabled.

Figure 5 shows heat maps of the die error in the X axis (left) and the Y axis (right) on the test panel. The right dies in the first two rows are marked red, indicating a die error around +100µm. The left dies of the third row are marked blue, indicating a die error around -100µm. Rows 4 and 5 are all green, meaning there is no shift in the X axis. Y errors show no large placement errors within the clusters. In the study, any die with an error of more than 15µm was marked as an outlier and discarded during site-by-site correction calculations.

Figure 6 shows the predicted X and Y residue values after correcting the die error using site-by-site exposure. The site-by-site exposure was run using the processed metrology data that was fed forward by the outlier control algorithm. The left side of the figure shows the residue values of most points are within ±3µm. The residue values for the rest of the points are around +100µm and -100µm, as expected. The right side of the figure shows that all data points have very small residue values in the Y axis, ±2µm. Figure 7 shows that the final predicted overlay yield is 85%, using site-by-site exposure with the overlay threshold set to ±15µm. Predicted residue values and yields are features of the feedforward system.

Following all the processes (feedforward metrology, site-by-site exposure and developing), actual overlay results for the test panel were measured with the offline metrology tool. The actual overlay results are shown in Figure 8 and Table 1. In the overlay heat map a blue dot indicates the overlay is within specification, in this case ±15µm. A red dot indicates the overlay is out of specification. The heat map matched predicted and expected results. Table 1 shows the overlay statistics of the good dies in the test panel; deviations in X and Y are less than 5µm, and all numbers are within the overlay threshold.

Table 2 compares the impact on yield and throughput of the various technologies we have described. With regular die-by-die lithography, the yield is 100%, but the throughput is only three panels per hour. With site-by-site lithography, the throughput increases to 32 panels per hour, but the yield drops to 40%. Adding outlier control technology and feedforward lithography increases throughput to 62.7 panels per hour and yield to 85%. The numbers will vary for different

	Average	Max	Min	Range	Std Dev
dx	1.04	2.20	-0.31	2.50	0.60
dy	0.25	1.40	-0.75	2.15	0.34

➤ Table 1. The statistics of good dies on the test panel. All the numbers are within ±2.5μm and the ±15μm overlay threshold.

	Features Used				Shot Number (ea)	Yield (%)	Throughput (pcs/hr)	Throughput Improved (%)
	Die by Die	Site by Site	Outlier Control	Feed Forward				
Condition 1	•				400	100	3	NA
Condition 2		•			25	40	32	966.67%
Condition 3		•	•		25	85	32	966.67%
Condition 4		•	•	•	25	85	62.6	1986.96%

➤ Table 2. Yield and throughput comparison table.

processes, but feedforward lithography and outlier control offer significant improvements in yield and throughput in this evaluation.

Summary

In the metrology data collected for this demonstration, the outliers showed large die errors compared to other nominal dies. The outlier control algorithm correctly identified all outliers using a customized threshold set to 20μm. Outliers were marked and discarded in the following exposure processes. The rest of the dies maintained good overlay. The outlier control technology worked as expected.

The study demonstrates the ability of outlier control technology and offline feedforward metrology to accurately identify outliers, eliminate their negative influence on site-by-site corrections and send optimized correction data to a lithography tool. It also shows that these technologies can be integrated to work together in a FOPLP process line.

Adding outlier control technology to site-by-site exposure boosted yield from 40% to 85%, and the combination of outlier control with off-line feedforward metrology increased throughput by approximately 20 times.

FURTHER READING

➤ [1] John Chang, Keith Best, Jian Lu, Burhan Ali, Mike Marshall, Rudolph Technologies, “Adaptive shot technology to address severe lithography challenges for advanced FOPLP,” ECTC, 2020.

➤ [2] Keith Best, John Chang, Mike Marshall, Jian Lu, Rudolph Technologies, “FOPLP lithography solutions to overcome die placement error, predict yield, increase throughput and reduce cost,” IWLPC, 2019.

➤ [3] Keith Best, Mike Marshall, Rudolph Technologies, “Advanced packaging metrology and lithography that overcomes FOWLP/FOPLP die placement error,” IWLPC, 2018.

➤ [4] Klaus Ruhmer, Rudolph Technologies, “Lithography challenges for 2.5D interposer manufacturing,” ECTC 2014, Orlando, FL.

➤ [5] Roger McCleary, “Panel-level advanced packaging,” ECTC 2015, Las Vegas, Nevada

➤ [6] K. Ruhmer, P. Cochet, and R. McCleary, “Panel-based fan-out packaging to reduce costs,” SMTA/Chip Scale Review International Wafer-Level Packaging Conference, San Jose California, Nov. 11-13, 2014.

➤ [7] K. Ruhmer, P. Cochet, R. McCleary, and N. Chen, “High-resolution patterning technology to enable panel-based advanced packaging,” IMAPS 2014, San Diego, California, October 13-16, 2014.