High Density, Tall Cu Pillars for 3D Packaging

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Abstract

With demands for shrinking footprints and increasing I/O of electronic components, there is an increasing interest in electrodeposited Cu pillar structures for Package on Package (PoP) interconnects. One example of interest involves a 3D package integration approach with the memory mounted above the processor for mobile applications. This paper will explore the processes required and discuss the challenges for Cu pillar fabrication of PoP interconnects at sub 100um pitches. The test vehicles will include variables such as pillar diameter and pitch for a 200um thick liquid film negative tone plating resist on a 300mm wafer format. The high-density pillar pitch is expected to present challenges to resist material applications, lithography capability, and plating capability. Work for this paper is supported by major material and tool suppliers for resist materials, lithography tools, and plating chemistries & plating tools.

JSR Micro, Rudolph Technologies, Atotech

Key words

Advanced Packaging, 2.5D, 3D, High Density Cu Pillar, TSV, Stepper, Electro-Plating, ECD, Cu Plating, Thick Resist

I. Introduction

Each advance in packaging technology brings new challenges for increased I/O and device integration. This has led to 2.5D and 3D, multi-dimensional packages or Package on Package (PoP) technologies [Figure 1]. PoP technology utilizes copper pillar bumps and through silicon via (TSV) to create interconnects between stacked memory chips and other integrated devices such as microprocessors. This paper investigates the requirements for lithography, photo material, and plating to create high density, tall copper pillars, 170µm in height, with a 45µm CD for a 4:1 aspect ratio with fine pitch of 65µm.

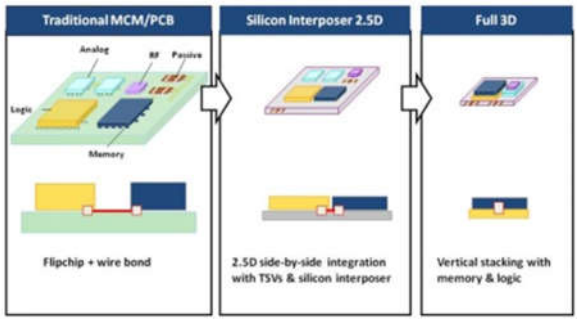

Figure 1

II. Enabling Technologies for High Density, Tall Copper Pillars

Copper pillars are electroplated into openings, that are imaged in thick layers of photoresist which are created by a photolithographic process. Current copper pillar technology and process is creating pillars ranging from 30-50µm in height, with aspect ratios from 1:1 to around 2:1.

Creating high-density copper pillars poses several process challenges for lithography, photo materials and electroplating. For lithography, the challenge is imaging vertical structures in thick photo material, and for photo material it is creating a thick, uniform film and for electroplating it is finding the balance of "current and deposition rate" required to fully fill the resist voids.

For copper pillar fabrication in thick photoresist, well controlled sidewall angles (SWA) are a critical requirement. This is especially true when electroplating high density tall copper pillars. Front-end exposure tools have high numerical aperture (NA) lenses with low depth of focus (DOF) that prevent adequate penetration of thick films with sufficient image contrast to achieve the side wall angle and resolution requirements. Mask aligners also struggle with high aspect ratio imaging, not because of their NA, but because they are unable to provide the necessary focus offset required to penetrate the film at high resolution, limiting their ultimate aspect ratio and side wall angle control. Although photoresist sidewall angles are primarily a function of the photoresist material and its processing (pre-bake, post-bake, developing, etc.), the exposure system still plays an important role. Accurate focus control across the wafer or substrate is required to achieve consistent and accurate CD control with straight and perpendicular side walls [1].

Figure 2

The lithography stepper employed in this study is a Rudolph Technologies JetStep® W2300 System (Figure 2). The JetStep® utilizes "on the

fly" focus control to ensure that every exposure is at the optimum focal plane height. This capability is essential when advanced packaging substrates become warped by film stress and thermal cycling. The system's lens, with a 0.1 numerical aperture (NA) provides a very large depth of focus (DOF) to maintain image integrity and CD control through thick films. This a priority for high aspect ratio imaging when films exceed 100µm. The system has the capability to provide variable wavelengths giving the user the ability to image at either "broadband" ghi-lines (365-436 nm), gh-lines (405-436 nm) or i-line (365 nm) wavelengths.

III. Experiment and Equipment Descriptions

Photoresist and Process

JSR THB-170N photoresist was chosen for this application. THB-170N is a negative tone photoresist designed for tall copper pillar plating applications. The polarity of the polymers of THB-170N is controlled to achieve high resolution, the cross-linker is optimized to control the cross-linking density and the photo-initiator is adjusted for better transparency from top to bottom enhancing the photoresist profile and resolution.

With new polymer, new cross-linker and new photo-initiator, THB-170N provided excellent coating performance, and also provided the fast photo-speed, development time and stripping time that conventional thick resist have not. While satisfying these performance aspects, the THB-170N also provided excellent plating performance for various solutions of Cu, Ni and Sn-Ag.

Comparing to the dry-film photoresist, which current resolution has only archived 70um CD in 180um thickness, the THB-170N is a liquid type spin-on photoresist with wide range thickness. The THB-170N is capable of single coating thicknesses up to 120µm and double coating up to 250µm. Further, resolutions of 20µm CD at 180µm film thickness have been achieved.

Lithography System and Process

A focus-exposure matrix (FEM) was first exposed to establish the exposure and focus parameters that would yield the best resolution results for plating. The wafer layout provided a large number of programmed focus and exposure conditions at a fixed stepping distance to enable quick and efficient characterization of the lithography process window [Figure 3].

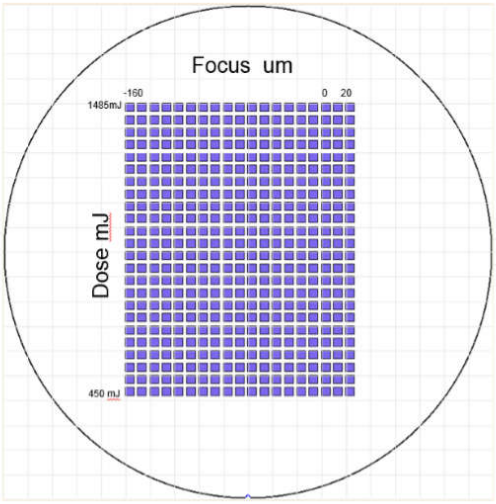

Figure 3

Based on the FEM results for this particular application and with the photoresist thicknesses near 200µm, a higher energy illumination of 1000mJ was required to image the thicker structures require for the copper pillars. Further broadband illumination (g,h,i wavelengths) was employed to maintain high throughput. The developing process employed 5-cycles with, 60 second spray and 60 second puddles using the industry standard TMAH 2.38% developer.

Reticle Imagery and Layout

A customized test reticle was fabricated to provide a range of CD and pitch dimensions [Figure 4].

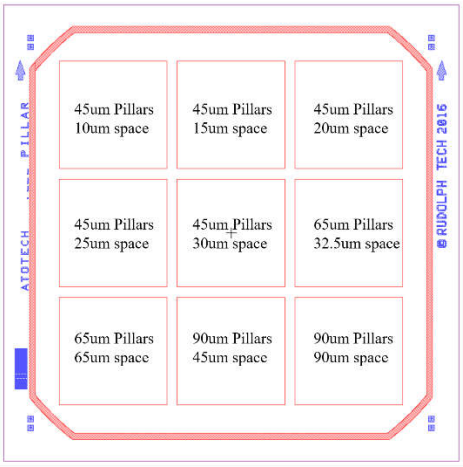

Figure 4

The target CD and pitch for this experiment was 45µm and 65µm respectively. A designed 20µm space was used between 45µm pillars to achieve the 65µm pitch [Figure 5].

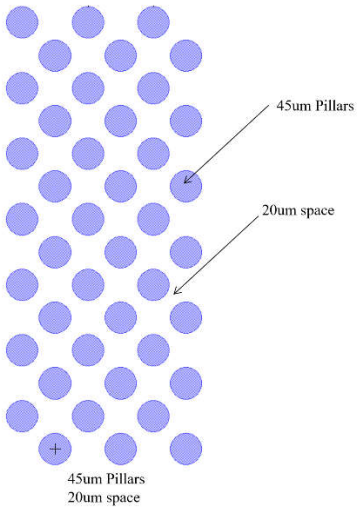

Figure 5

Electroplating System and Process

Perhaps one of the most challenging ECD applications for both quality and throughput efficiency is bottom up plating of high aspect ratio pillar structures that can be used to meet increasing I/O requirements (decreasing pitch) for 3D applications. Figure 6, from simulations, highlights one of one of the challenges for plating high aspect ratio pillars and shows limited fluid exchange (green) at the bottom of the pillar structure [2].

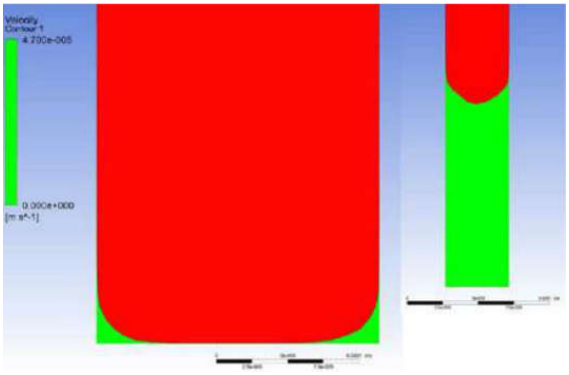

Figure 6

When starting initial investigations with regard to optimization of a system for plating high aspect ratio pillars, it was obvious that a significant obstacle existed with available technology to provide a suitable test vehicle. Given that this technology was not yet mature or commercially available, there were no “off the shelf” resources known to provide the critical dimensions and resist thicknesses desired for plating development. The primary goal for this paper was not to establish an optimum POR for commercial plating, but rather to provide copper filled pillar structures for evaluation of the resist quality and determine if an ultra-high thick wet film resist process offered promise for further development.

The method to evaluate resist structures on silicon wafers consisted of a cleaving technique followed by SEM evaluation. This method suffices for lower aspect ratio structures with much thinner resists, but as we have observed

with thick resist and high aspect ratios, cleaving may not provide an accurate measure of the plating resist quality due to distortion of the resist during sample preparation [Figure 7].

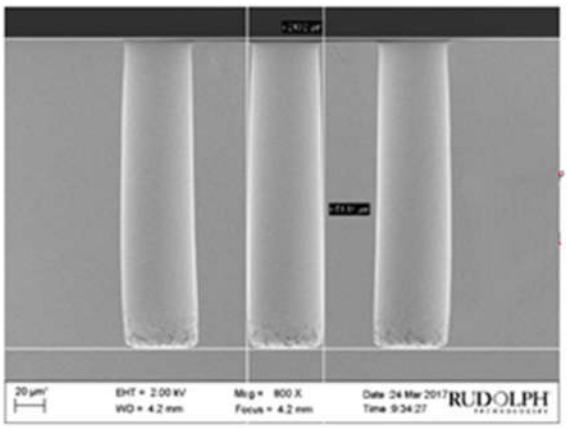

Figure 7

Experimental method

(4) 300mm patterned wafers were provided by Rudolph, with JSR resist coated at (2) different resist thicknesses. The seed layer was Ti/Cu on silicon and provided by JSR. Given the limited sample quantity, the wafers were segmented into sections and plated in coupon format in an advanced ECD Multiplate test cell [Figure 8], commercially available for wafer and panel formats. Pretreatment prior to electrolytic plating included descum (O2 Plasma, 0.2 bar), evacuation (3 cycles, 20 mbar), and Spherolyte cleaner 3 for 30 seconds.

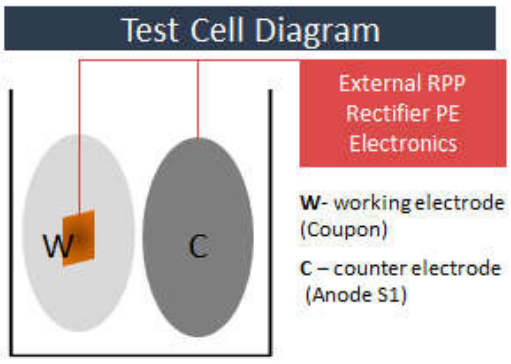

Figure 8

The Atotech Multiplate tool is equipped with technical features that enable optimal electrolyte flow, programmable agitation, and reverse pulse plating at very high-current densities [Figure 9]. For this exercise, the operating temperature, copper electrolyte content, and the acid concentration were optimized for defect-free plating of high aspect ratio pillars[3].

Figure 9

Plating conditions including current density and flow rate were purposely conservative, so no defects or anomalies would skew the evaluation of the resist quality. A two additive (accelerator and suppressor) system is employed as compared to a traditional three additive suite. The absence of a strong leveler minimizes the risk of organic co-deposition of the additives, leading to fewer voids. For optimization of the profile of the pillar, deposit height uniformity, and maximum current density, larger sample quantities is required, and were not a focus at this time, but will be considered for future publication based on works in progress.

IV. Exposure and Plating Results

Initially, plating of 150µm tall Cu pillar was targeted including a pillar structure with 90µm diameter, a resist height of 200µm, with a minimum pitch of 135µm. The resulting deposition speed of 2.8µm per minute was used

for the resist aspect ratio of 2.2:1 [Figures 10, 11, 12].

Pillar diameter	90um
Resist height	200um
Pitch (offset min)	135um
Aspect Ratio	2.2:1
Tool	Multiplate Test Cell
Electrolyte	Sperolyte Cu MPX
VMS	CB 50 CT
Temp	40°C
Plating Recipe	10 Step PRP
Time	52 minutes
Plating Current Density	13 ASD
Plating height	147um
Deposition Rate	2.8um/min

Figure 10

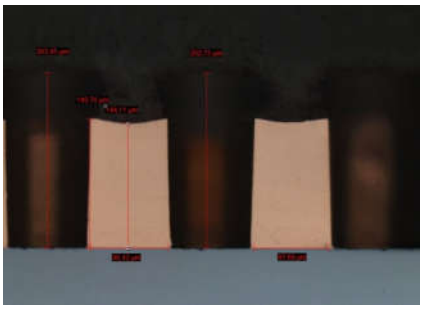

Figure 11

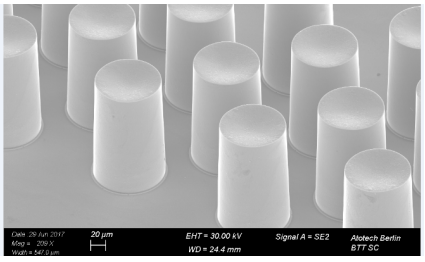

Figure 12

After the promising results were achieved for the larger resist geometries of 90µm x 200µm, tests that targeted smaller feature sizes were conducted. The results showed pillar structures reflective of excellent resist mold profiles, with 170µm of Cu deposited into a resist height of 180µm. Pillar diameter was 45µm, with a minimum pitch of 65µm and a deposition speed of 1.9µm per minute for the resist aspect ratio of 4:1 [Figures 13, 14, 15].

Pillar diameter	45um
Resist height	180um
Pitch (offset min)	65um
Aspect Ratio	4:1
Tool	Multiplate Test Cell
Electrolyte	Sperolyte Cu MPX
VMS	CB 50 CT
Temp	40°C
Plating Recipe	10 Step PRP
Time	88 min
Plating Current Density	8.5 ASD
Plating height	170um
Deposition Rate	1.9um/min

Figure 13

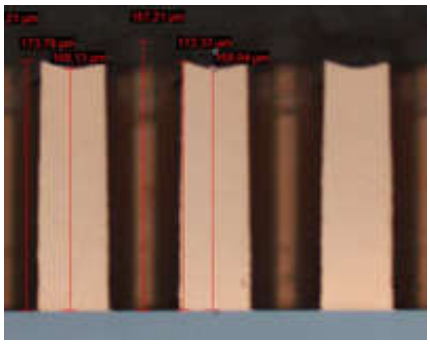

Figure 14

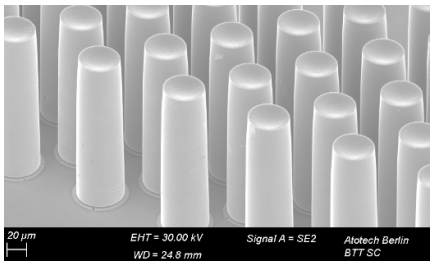

Figure 15

V. Conclusion

The results of this study show high-density, tall copper pillars up to 170µm with aspect ratios greater than 4:1 are feasible. For plating, these feasibility samples show promising results for resist quality and profile. An ultra-high thick wet

film resist can be considered for the ongoing plating development of high aspect ratio pillar structures.

Acknowledgement

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